REMARKS

Prior to applicants' invention, there existed a need for a device that ensured restricted access of programs and/or data to authorized computer systems while preserving user privacy. In response to that need, applicants devised the microprocessor of amended claim 1, which includes: (1) an identifier that identifies the microprocessor, and (2) embedded instructions for comparing a hash value, derived from the identifier and a key, to an expected hash value.

The claimed microprocessor enables a server to authenticate a computer system (that includes the claimed microprocessor) by sending a key and an expected hash value to the computer system, then waiting for a response that indicates whether a hash value that the microprocessor generates matches the expected hash value. The microprocessor includes microcode for generating that hash value from the key and an identifier contained within the microprocessor, then comparing it with the expected hash value that the server provided. In a significant departure from prior authentication processes, the claimed microprocessor itself — not the server or other components contained within the computer system — performs the hash value comparison operation prior to providing the result to the server.

Rejection Under 35 U.S.C. §102 Based on Mi et al.

The examiner rejected claims 1-6 under 35 U.S.C. §102(e) as being anticipated by Mi et al. In response, applicants amended claims 1 and 2 by adding to them from now canceled claim 4 the requirement that the embedded instructions comprise microcode.

Mi does not anticipate the microprocessor of claims 1-3, and 5-6, as amended. The microprocessor of claim 1 comprises (1) an identifier that identifies the microprocessor, and (2) embedded instructions for comparing a hash value, derived from the identifier and a key, to an expected hash value. As

Mi does not anticipate the microprocessor of claims 1-3, and 5-6, as amended. The microprocessor of claim 1 comprises (1) an identifier that identifies the microprocessor, and (2) embedded instructions for comparing a hash value, derived from the identifier and a key, to an expected hash value. As amended, claim 1 requires that those embedded instructions comprise microcode. Although Mi describes a microprocessor that includes an identifier that identifies the microprocessor, Mi does not describe a microprocessor that includes embedded instructions for comparing a hash value, derived from the identifier and a key, to an expected hash value. Nor does Mi describe a microprocessor that includes embedded instructions that comprise microcode for performing such a hash value comparison operation.

Although Mi mentions that embedded information for identifying a processor may be stored in a constant ROM that holds data that microcode instructions may use, Mi does not describe a microprocessor that includes microcode for performing a hash value comparison operation. In response to a previous office action, applicants enclosed copies of U.S. Patents 5,790,834 and 5,794,066 (which Mi references) that confirm Mi describes nothing more than microcode instructions for enabling an application to access a processor number. Mi does not indicate or suggest that the microprocessor Mi describes also includes microcode for performing a hash value comparison operation. Because Mi does not describe a microprocessor with embedded instructions that comprise microcode for performing a hash value comparison operation, Mi does not anticipate the microprocessor of amended claim 1.

Nor does Mi anticipate the microprocessor of claim 2, as amended. Because amended claim 2 depends upon amended claim 1, Mi fails to anticipate the microprocessor of amended claim 2 for that reason alone. Mi does not anticipate that claim for another reason. Amended claim 2 further specifies that the microprocessor includes embedded instructions for producing a hash value that is a function of the identifier and a key. Like amended claim 1, amended claim 2 specifies that the embedded instructions comprise microcode. In addition to failing to describe a microprocessor with microcode for performing a hash value comparison function, Mi fails to describe a microprocessor with microcode for performing a hash value generation operation. Because Mi does not describe a microprocessor with embedded instructions that comprise microcode for performing a hash value generation operation, Mi does not anticipate the microprocessor of amended claim 2 for this additional reason.

Because claims 3, 5 and 6 depend (directly or indirectly) upon amended claim 1 or amended claim 2, Mi cannot anticipate those claims either. Because MI does not describe a processor that anticipates the processor of applicants' claims 1-3, and 5-6, applicants respectfully request the examiner to withdraw the rejection of those claims based upon that reference.

Rejection Under 35 U.S.C. §102 Based on Pearce et al.

The examiner rejected claims 12-13, 15-16 and 20 under 35 U.S.C. §102(e) as being anticipated by Pearce et al. Applicants have canceled claims 12-13, 15-16 and 20, obviating the need to respond to this rejection.

Rejection Under 35 U.S.C. §103 Based on Pearce and Matsumoto

The examiner rejected claim 14 under 35 U.S.C. §103(a) as being unpatentable over Pearce in view of Matsumoto. Applicants have canceled claim 14, obviating the need to respond to this rejection.

Conclusion

Because Mi does not describe the microprocessor of applicants' claims 1-3, and 5-6, applicants respectfully request the examiner to withdraw the rejection of those claims based on that reference, and to allow them to issue.

Respectfully submitted,

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Mark Seeley
Reg. No: 32,299
ATTORNEY FOR APPLICANT

Intel Corporation
Mail Stop SC4-202
2200 Mission College Blvd.
Santa Clara, CA 95052-8119
(408) 765-7382

CERTIFICATE OF TRANSMISSION

(37 C.F.R. § 1.8(a))

I hereby certify that this correspondence is being transmitted by facsimile to the United States Patent and Trademark Office on September 14, 2004.

Mark Seeley
Name of Person Sending Facsimile

Mark Seeley
Signature